What is Claimed is:

[c1] Data transmission system having a plurality of Local Area Networks (LANs) interconnected by a hub including a plurality of LAN adapters respectively connected to the plurality of LANs, the data transmission system comprising:

a packet switch interconnecting the plurality of LAN adapters wherein a packet transmitted by any one of the plurality of LAN adapters to the packet switch includes a header containing at least the address of the adapter to which the packet is forwarded, the packet switch includes a plurality of input ports and a corresponding plurality of output ports both being respectively connected to the plurality of LAN adapters, each pair of input port and output port defining a cross point;

the packet switch comprises:

a memory block located at each cross point for storing any data packet which is received from the input port corresponding to the cross point and which is to be forwarded to the output port corresponding to the cross point, and

a scheduler associated with each output port for selecting at each clock time a memory block among all memory blocks corresponding to the output port and causing the memory block to forward the stored data packet to the output port when predetermined criteria are met.

[c2] Data transmission system according to claim 1, wherein the memory block located at each cross point of the switch module includes a data memory unit for storing at least a data packet and a first memory controller which determines from the header of the received data packet whether the packet is to be forwarded to the output port associated with the cross point and for storing the data packet into the data memory unit in such a case.

[c3] Data transmission system according to claim 2, wherein the memory block includes a header validation control block for determining whether the header of a data packet received from the input port contains the address of the output port associated with the cross point and the first memory controller which stores the data packet into the data memory unit if the header contains the address of the output port and for reading the data packet to forward it to the

output port.

[c4] Data transmission system according to claim 3, wherein the scheduler sends a validation signal to the header validation control block to authorize the first memory controller to store the data packet into the data memory unit.

[c5] Data transmission system according to claim 4, further comprising an output data block connected to each output port which stores a data packet received from any memory block and transmits the data packet to the output port under the control of the scheduler.

[c6] Data transmission system according to claim 5, wherein the output data block includes a data selection block which validates the data packet after receiving a validating signal from the scheduler, an output memory unit which stores the data packet and a second memory controller which controlls the operation of storing the data packet into the output memory unit and the operation of reading the output memory unit for transmitting the data packet to the output port.

[c7] Data transmission system according to claim 6, wherein the packet switch includes a plurality of switch modules and wherein each down switch module includes for each output port an input expansion data block for buffering a data packet received from an expansion bus in connected to an up switch module and corresponding to the same output port as the output port of the down switch module.

[c8] Data transmission system according to claim 7, wherein the input expansion data block includes an expansion memory unit which buffers the data packet received from the expansion bus in, a header validation block which determines whether the header of the data packet contains the address of the output port associated with the cross point, and a third memory controller which stores the data packet into the expansion memory unit and reads the expansion memory unit to forward the data packet to the output port of the down switch module.

[c9] Data transmission system according to claim 8, wherein the scheduler sends a validation signal to the header validation block to authorize the third memory

controller to store the data packet into the expansion memory unit.

[c10] Data transmission system according to claim 1, wherein an overflow signal is sent by the memory block to the scheduler when the memory block overflows.

[c11] Data transmission system according to claim 10, further comprising an overflow bus to transport the data packet to the memory block corresponding to the output port that after the scheduler has prevented the data packet from being stored into the memory block which overflows and has selected and validated another memory block which does not overflow.

[c12] Data transmission system according to claim 10, further comprising a back-pressure mechanism which sends back-pressure signals to input adapters to request the input adapters to reduce the flow of the data packets transmitted to the packet switch when there is too much overflow detected by each scheduler of the packet switch.

[c13] Data transmission system according to claim 12, further comprising an overflow mechanism adapted to receive overflow control signals from the schedulers of the packet switch when there is too much overflow and to transmit an overflow signal to the back-pressure mechanism.

[c14] Data transmission system according to claim 1, wherein the header of the data packet includes two bytes in which the first byte contains an identification field (unicast, multicast) and the second byte contains a module address field when the packet switch comprises several packet switch modules.